Stereo Vision IP Suite

Compact size and Low latency,
For Intel® (former Altera) FPGAs stereo vision IP
(Tokyo Institute of Technology with FUJISOFT Inc.)

Feature

- Processing of higher frame rate than MPU/DSP (supports 720p/30 fps)
- The unique algorithm for “Rectification and Distortion Correction” with compact logical size
- Achieve the stereo processing compactly with adopting SAD
- The Object Recognition/tracking performed by the disparity information at the same time
- Automatic Calibration corrects the deviation of the camera position that is caused by many factors such as vibration, temperature, etc. which changes over time.

Block Diagram

Cyclone® V SoC FPGA

HPS Block
(ARM® Cortex-A9 dual core)

Automatic Calibration

Object Tracking

R-Camera

L-Camera

Image Sensor I/F

Rectification Distortion Correction

Stereo Matching

Object Detection

Application Viewer
**Evaluation Version IP Installed and Pre-Installed Stereo Vision.**
You can also try immediately the stereo image viewer on the PC included!

### Specification of Stereo Vision Evaluation Kit

<table>
<thead>
<tr>
<th>Item</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base Line</td>
<td>100 mm, 149 mm, 198 mm</td>
</tr>
<tr>
<td>Image Size</td>
<td>1280 (H) x 720 (V)</td>
</tr>
<tr>
<td>Frame Rate</td>
<td>30 fps</td>
</tr>
<tr>
<td>View Angle</td>
<td>Approx. 42°</td>
</tr>
<tr>
<td>Disparity Search Range</td>
<td>256 pixels</td>
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</table>
| Resolution of Distance Detection | Theoretical value: The maximum distance to get the resulting distance information when the ideal images entered.  
Base Line: 100 mm Approx. 640 mm—Approx. 165 m Approx. 2.2% (1)  
Base Line: 149 mm Approx. 960 mm—Approx. 245 m Approx. 1.5% (1)  
Base Line: 198 mm Approx. 1300 mm—Approx. 330 m Approx. 1.1% (1) |
| Distance Accuracy | 1 When the distance measurement of 30m destination |
| Latency | Until IP output part: Approx. 2 ms (From input of Rectification & Distortion IP to Stereo Matching IP) |
| Output Image | L/R Camera Image  
Image after L/R Rectification & Distortion  
Disparity Image  
Each 8 bit  
Each 8 bit  
12 bit (Integral 8 bit, Decimal 4 bit) |
| Output I/F | Gigabit Ethernet |
| FPGA Use Resources | ALMs: 25.6 K (LE: 67.7 K), RAM: 3.1 M bit  
[Detail] Image Input IF 0.5 K ALMs (1.3 K LE)  
Rectification & Distortion IP 1.5 K ALMs (4.0 K LE)  
Stereo Vision 7.4 K ALMs (19.6 K LE)  
Object Detection 10.7 K ALMs (28.3 K LE) |

### Delivers

- **Hardware**
  - Terasic, DE1-SoC Board  
  - Terasic, D5M Digital Camera Package  
  - Cameras are calibrated.  
    * Prepare multiple type base line (100mm, 149mm, 198mm) (2)  
    * Aluminium Board for fixing L/R Camera (2)  
    * Connection Cable, AC adapter |
- **Software**
  - Application for Sample Demo (For ARM, Source code provided)  
  - Linux Kernel 3.16, distribution (Binary provided)  
  - Sample Driver for IP Core Control (Source Code, Part of Binary provided)  
  - Camera Image Viewer (Windows7 Source Code provided) (3) |
- **Document**
  - Start-up Guide for the Evaluation Kit  
  - User's Manual for IP Core  
  - Q&A for IP, Evaluation Kit (In 3 months, by 20H)  
  - Customizing for Purchaser (Extra charge)  
  - OS Supporting (Extra charge)  
  - Platform and tripod for fixing cameras are NOT installed in the Evaluation Kit.  
  - The PC operation for the viewer application needs to Gigabit Ethernet corresponding LAN port. The LAN crossover cable for connection is NOT included in the Evaluation Kit.  

### Contact

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