FUJISOFT
creating new values

Stereo Vision IP Suite

Compact size and Low latency, For Intel® (former Altera) FPGAs stereo vision IP

(Tokyo Institute of Technology with FUJISOFT Inc.)

To safe driving assistance (ADAS)

To detect the intruder

To detect the customer flow line in the store

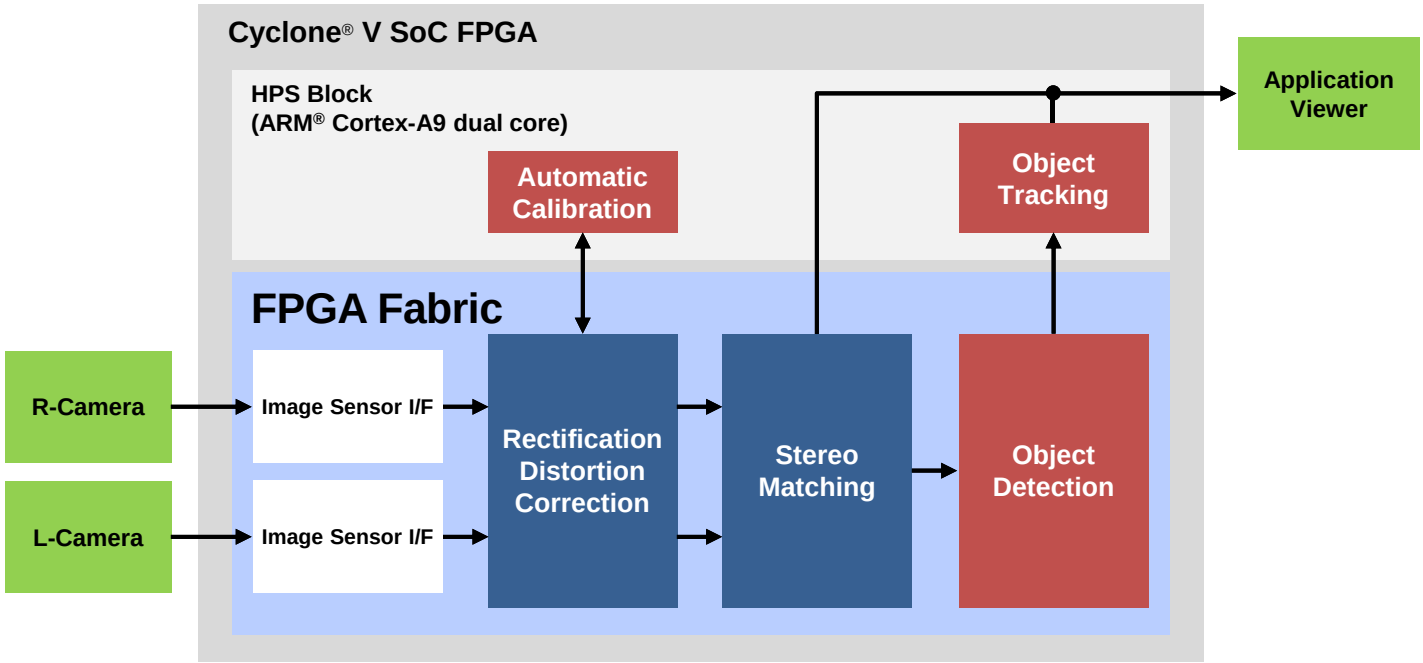
To detect ruts on the road automatically

Feature

- ✓ **Processing of higher frame rate than MPU/DSP (supports 720p/30 fps)**
- ✓ **The unique algorithm for “Rectification and Distortion Correction" with compact logical size**
- ✓ **Achieve the stereo processing compactly with adopting SAD**
- ✓ **The Object Recognition/tracking performed by the disparity information at the same time**
- ✓ **Automatic Calibration corrects the deviation of the camera position that is caused by many factors such as vibration, temperature, etc. which changes over time.**

※ Automatic Calibration function performs for installed type Camera only

Block Diagram

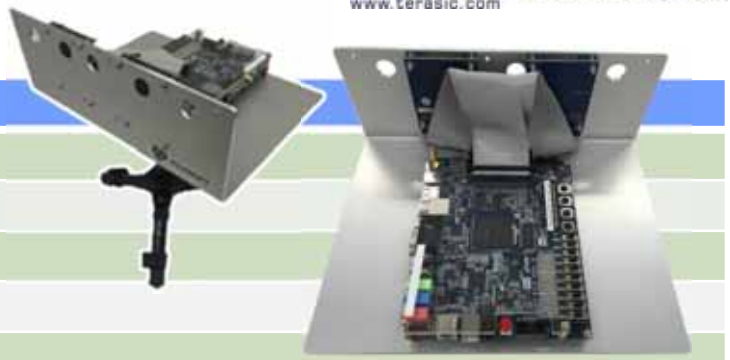


FPGA Design Solutions Network
FUJISOFT

Stereo Vision Evaluation Kit

EVALUATION VERSION IP INSTALLED AND PRE-INSTALLED STEREO VISION.
YOU CAN ALSO TRY IMMEDIATELY
THE STEREO IMAGE VIEWER ON THE PC INCLUDED!

terasIC www.terasic.com Terasic Technologies Inc.



Specification of Stereo Vision Evaluation Kit

Item	Specification
Base Line	100 mm, 149 mm, 198 mm
Image Size	1280 (H) x 720 (V)
Frame Rate	30 fps
View Angle	Approx. 42°
Disparity Search Range	256 pixels
Range of Distance Detection Distance Accuracy	**Theoretical value**：The maximum distance to get the resulting distance information when the ideal images entered. Base Line： 100 mm　Approx. 640 mm～Approx. 165 m　Approx. 2.2% (※1) Base Line： 149 mm　Approx. 960 mm～Approx. 245 m　Approx. 1.5% (※1) Base Line： 198 mm　Approx. 1300 mm～Approx. 330 m　Approx. 1.1% (※1) ※1 When the distance measurement of 30m destination
Latency	Until IP Output part：Approx. 2 ms（From Input of Rectification & Distortion IP to Stereo Matching IP）
Output image	L/R Camera Image　Each 8 bit Image after L/R Rectification & Distortion　Each 8 bit Disparity Image　12 bit (Integral 8 bit, Decimal 4 bit)
Output I/F	Gigabit Ethernet
FPGA Use Resources	ALMs：25.6 K (LE：67.7 K), RAM: 3.1 M bit [Detail] Image Input IF 0.5 K ALMs (1.3 K LE)　Rectification & Distortion IP 1.5 K ALMs (4.0 K LE) Stereo Vision 7.4 K ALMs(19.6 K LE)　Object Detection 10.7 K ALMs (28.3 K LE) Others 5.0 K ALMs (13.2 K LE)

Deliverables

◆Hardware

- Terasic, DE1-SoC Board
  Cyclone® V SX SoC 5CSEMA5F31C6 Installed
- Terasic, D5M Digital Camera Package
  5 million Pixel CMOS Installed
  1280 x 720@30 fps / 640 x 480@60 fps,
  1920 x 1080@15 fps (※1)
- Cameras are calibrated.
  * Prepare multiple type base line
  (100mm, 149mm, 198mm) (※1)
- Aluminium Board for fixing L/R Camera (※2)
  (Prepare screw hole for Camera platform mounting)
- Connection Cable, AC adapter

◆Software

- Application for Sample Demo (For ARM. Source Code provided)
- Linux Kernel 3.16, distribution (Binary provided)
- Sample Driver for IP Core Control (Source Code, Part of Binary provided)
- Camera Image Viewer (Windows7 Source Code provided) (※3)

◆Document

- Start-up Guide for the Evaluation Kit
- User's Manual for IP Core

※1 Choose one combination of base line and pixel when ordered.
(Modification of pixel will be supported by our support team.)
※2 Platform and tripod for fixing cameras are NOT installed in the Evaluation Kit.
※3 The PC operation for the viewer application needs to Gigabit Ethernet corresponding LAN port. The LAN crossover cable for connection is NOT included in the Evaluation Kit.

Supports

- Q&A for IP, Evaluation Kit（In 3months, by 20H)
- Customizing for Purchaser（Extra charge)
- OS Supporting（Extra charge)

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